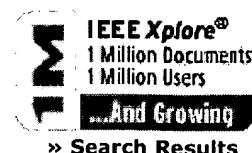




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#### 3 Realization of a mixed-mode neural coprocessor for signal processing

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Cleary, R.T.; Zayac, M.P.;

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**5 Design of a hybrid digital-analog neural co-processor for signal processing**

*Romariz, A.R.S.; Ferreira, P.U.A.; Campelo, J.V., Jr.; Graciano, M.L., Jr.; da Costa, J.C.;*

EUROMICRO 96. 'Beyond 2000: Hardware and Software Design Strategies'.  
Proceedings of the 22nd EUROMICRO Conference , 2-5 Sept. 1996

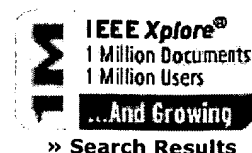
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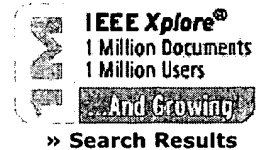
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Computational Science and Engineering, IEEE [see also Computing in Science &amp; Engineering], Volume: 4, Issue: 1, Jan.-March 1997

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[\[Abstract\]](#)   [\[PDF Full-Text \(116 KB\)\]](#)   **IEEE JNL****2 Realization of a mixed-mode neural coprocessor for signal processing***Romariz, A.R.S.; Ferreira, P.U.A.; Campelo, J.V., Jr.; Graciano, M.L., Jr.; Maia, O.R., Jr.; da Costa, J.C.;*

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[\[Abstract\]](#)   [\[PDF Full-Text \(80 KB\)\]](#)   **IEEE CNF****3 Design of a hybrid digital-analog neural co-processor for signal processing***Romariz, A.R.S.; Ferreira, P.U.A.; Campelo, J.V., Jr.; Graciano, M.L., Jr.; da Costa, J.C.;*

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**5 Simulating shared memory in message passing model***Aguilar, O.R.; Datta, A.K.; Ghosh, S.;*

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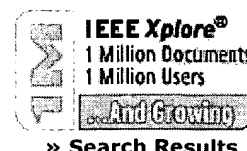
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